THE CLAIMS

Claims 1-42 are pending in the instant application. The Applicant requests reconsideration of the claims in view of the following remarks.

Listing of claims:

1. (original) A system for an integrated set-top box, the system comprising:

a single integrated circuit chip comprising:

a first satellite receiver demodulator integrated within said single integrated circuit chip;

at least a second satellite receiver demodulator integrated within said single integrated circuit chip; and

at least one processor integrated within said single integrated circuit chip and coupled to said first satellite receiver demodulator and said second satellite receiver demodulator.

2. (original) The system according to claim 1, wherein said at least one processor comprises a MIPS processor, a floating point processor and at least one data transport processor.

3. (Previously Presented) The system according to claim 1, comprising a programmable memory integrated within said single integrated circuit chip.

4. (original) The system according to claim 3, wherein said programmable memory stores at least one of security information and configuration information for said single integrated circuit chip.

5. (original) The system according to claim 4, wherein said security information comprises at least one of a security key and a device identifier (ID)

6. (original) The system according to claim 5, wherein said device identifier comprises at least one of an electronic serial number and an address.

7. (original) The system according to claim 4, wherein said configuration information comprises at least one of configuration data and code for configuring said single integrated circuit chip.

8. (original) The system according to claim 3, wherein said programmable memory is a one-time programmable memory.

9. (Previously Presented) The system according to claim 1, comprising at least one video decoder integrated within said single integrated circuit chip and coupled to said at least one processor.

10. (original) The system according to claim 9, wherein said at least one video decoder is a standard definition MPEG-2 video decoder.

11. (Previously Presented) The system according to claim 9, comprising at least one video and graphics display engine integrated within said single integrated circuit chip and coupled to said at least one video decoder.

12. (Previously Presented) The system according to claim 11, comprising at least one video encoder integrated within said single integrated circuit chip and coupled to said at least one video and graphics display engine.

13. (Previously Presented) The system according to claim 12, comprising at least one video digital-to-analog converter and RF modulator integrated within said single integrated circuit chip and coupled to said at least one video encoder.

14. (Previously Presented) The system according to claim 1, comprising at least one audio decoder integrated within said single integrated circuit chip and coupled to said at least one processor.

15. (original) The system according to claim 14, wherein said at least one audio decoder is an MPEG-2 audio decoder.

16. (Previously Presented) The system according to claim 14, comprising at least one audio digital-to-analog converter integrated within said single integrated circuit chip and coupled to said at lest one audio decoder.

17. (Previously Presented) The system according to claim 1, comprising at least one memory controller integrated within said single integrated circuit chip and

coupled to at least said at least one processor.

18. (original) The system according to claim 17, wherein said at least one memory controller comprises a unified dual data rate DRAM memory controller.

19. (Previously Presented) The system according to claim 1, comprising a digital satellite equipment control (DiSEqC) bus integrated within said single integrated circuit chip.

20. (Previously Presented) The system according to claim 1, comprising at least one of a plurality of peripheral interfaces comprising, an infrared interface, a universal asynchronous receiver/transmitter, a serial peripheral interface, a binary synchronous communication interface, general purpose input/output pins, and pulse width modulation controller interface, integrated within said single integrated circuit chip.

21. (Previously Presented) The system according to claim 1, comprising at least one read-only memory integrated within said single integrated circuit chip..

22. (original) The system according to claim 21, wherein said at least one read-only memory comprises a CPU boot ROM and a FLASH.

23. (Previously Presented) The system according to claim 1, comprising at least one debug port integrated within said single integrated circuit chip.

24. (original) The system according to claim 23, wherein said debug port comprises a JTAG port or any variation thereof.

25. (Previously Presented) The system according to claim 1, comprising at least one card reader or writer interface integrated within said single integrated circuit chip.

26. (original) The system according to claim 25, wherein said card reader or writer interface is a smart card reader or writer interface.

27. (Previously Presented) The system according to claim 1, comprising at least one core voltage regulator integrated within said single integrated circuit chip.

28. (Previously Presented) The system according to claim 1, comprising at least one phase lock loop integrated within said single integrated circuit chip.

29. (Previously Presented) The system according to claim 1, comprising at least one telephony modem integrated within said single integrated circuit chip.

30. (original) The system according to claim 1, wherein said first satellite receiver demodulator and said second satellite receiver demodulator are at least one of 8 PSK, 8 PSK-turbo and QPSK demodulators.

31. (original) A method for processing information in a set-top box, the system comprising:

receiving a first modulated signal by a first satellite receiver within a single integrated circuit chip;

demodulating said first modulated signal by said first satellite receiver within said single integrated circuit chip to generate a first demodulated signal;

receiving a second modulated signal by a second satellite receiver within said single integrated circuit chip; and

demodulating said second modulated signal by said second satellite receiver within said single integrated circuit chip to generate a second demodulated signal.

32. (Previously Presented) The method according to claim 31, comprising decoding within said single integrated circuit chip, a video portion of said first demodulated signal to generate a first decoded video signal.

33. (Previously Presented) The method according to claim 32, comprising encoding within said single integrated circuit chip, said first decoded video signal within said single integrated circuit chip to generate a first encoded digital video signal.

34. (Previously Presented) The method according to claim 33, comprising converting within said single integrated circuit chip, said first encoded digital video signal to a first analog video signal.

35. (Previously Presented) The method according to claim 31, comprising decoding within said single integrated circuit chip, an audio portion of said first demodulated signal to generate a first decoded digital audio signal.

36. (Previously Presented) The method according to claim 35, comprising converting within said single integrated circuit chip, said first decoded digital audio signal to a first analog audio signal.

37. (Previously Presented) The method according to claim 31, comprising decoding within said single integrated circuit chip, a video portion of said second demodulated signal to generate a second decoded video signal.

38. (Previously Presented) The method according to claim 37, comprising encoding within said single integrated circuit chip, said second decoded video signal within said single integrated circuit chip to generate a second encoded digital video signal.

39. (Previously Presented) The method according to claim 38, comprising converting within said single integrated circuit chip, said second encoded digital video signal to a second analog video signal.

40. (Previously Presented) The method according to claim 37, comprising decoding within said single integrated circuit chip, an audio portion of said second demodulated signal to generate a second decoded digital audio signal.

41. (Previously Presented) The method according to claim 40, comprising converting within said single integrated circuit chip, said second decoded digital audio signal to a second analog audio signal.

42. (original) The method according to claim 31, wherein said demodulating of said first modulated signal and said demodulating of said second modulated signal occurs simultaneously.